REMARKS

Claims 1, 3-11, and 14 were rejected under §112, second paragraph, and have been amended as to form (they now refer to one pad). Reconsideration and withdrawal of the rejection are respectfully requested.

Claims 1, 3-11, 14, and 42-49 were rejected as anticipated by KER et al. 2001/0010408. Reconsideration and withdrawal of the rejection are respectfully requested.

KER et al. do not disclose the barrier metal of claim 1. There is no reference to any barrier metal between the bonding pad (e.g., 250 in Figure 4) and the metal layer beneath the bonding pad (e.g., 240 in Figure 4).

KER et al. also do not disclose that the lower copper layer is not electrically connected to the upper copper layer as in claim 1. The Official Action points to the separation between metal layer 210 and metal layer 240 in Figure 4. However, as shown in Figure 3 and as explained in paragraphs 0035 and 0037, all of the metal layers 210, 220, 230, 240, and 250 are electrically connected to each other in series with vias (214, 224, 234, 244).

Accordingly, claims 1, 3-11 and 14 avoid the rejection under §102.

Dependent claim 4 further avoids the rejection because KER et al. do not disclose that the copper area ratio of the metal layer 240 is at least 70%. At paragraph 0033, KER et al.

state that the width of the metal layers 210, 220, 230, and 240 should be as small as possible to reduce the amount of substrate 200 overlapped by these layers. The reference provides no dimensions from which the claimed area ratio can be determined. The drawings (see, for example, Figure 7) show that the area ratio of these layers is less than 50%, assuming that these are drawn to scale (which is not a good assumption given that the widths are to be as small as possible). There is no basis for stating that the reference discloses that the area ratio of these layers is at least 70%.

With regard to claim 42, KER et al. do not disclose that the copper layer under the bonding pad and in electrical contact therewith, is electrically isolated from one of the copper interconnect layers at the first level. Figure 23 appears to show that layers 54 and 53 are not electrically connected to anything; however as stated in paragraph 0051, all of the layers 51-56 are connected with via plugs that are "not shown." Indeed, the arrangement is similar to that of Figures 3-6 where all of the metal layers are electrically connected. Paragraph 0051 further provides that the via plugs should not be under the bonding pad opening 82, which helps explain why the connections are not shown in Figure 23, which is concerned with the area under the bonding pad.

A feature of claim 41 is that: "one of said copper interconnect layers at said first level being elongated from said

internal circuit region to said bonding region under said copper layer in electrical isolation therefrom." Namely, in the semiconductor device according to claim 41, the copper interconnect layer is elongated from the internal circuit region to the region under the bonding region (see the description of the present invention, page 6, lines 13-18). Such a feature is not described in the cited reference.

Accordingly, claims 42-49 avoid the rejection under §102.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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